UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,738	01/25/2002	Gilbert Wolrich	10559-618001/P12857	2797

20985 7590 12/17/2007

FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

MAIL DATE	DELIVERY MODE
12/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/057,738	WOLRICH ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2007 and 06 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,13,16-21,26-29,33-35,37,40,41,43-45,49-51 and 53-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13,16-21,26-29,33-35,37,40,41,43-45,49-51 and 53-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/16/07 and 9/13/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed on 10 October 2007. Claims 1-7, 13, 16-21, 26-29, 33-35, 37, 40, 41, 43-45, 49-51 and 53-61 are pending. All objections and rejections not repeated below are withdrawn.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 16 July 2007 and 13 September 2007 were filed after the mailing date of the Application on 25 January 2002. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 13, 49, 55, 56 and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by Correale, Jr. et al. [US 6,587,905 B1] (hereinafter "Correale").

Per claims 13, 49, 55, 56 and 61, Correale teaches a data processor (see Correale, claim 4, "a data processing system", the processor is considered to be including the CPU, other Master devices, and the PLB Arbiter) comprising:

a plurality of programming engines (see Fig. 10, the Master devices);

a push arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of an unidirectional push bus (see Fig. 10, rdDBus) by a plurality of external memory resources that are external to the data processor (see Fig.10, the Slave devices), the push bus arbiter being internal to the data processor (see col. 4, lines 1-6, PLB and its arbiter are comprised within the processor architecture), the push bus to push data from the memory resources to an input transfer memory (not clearly shown by Correale in its drawings, but it is clear that a register must be present on a processor's input port which is connected to a data bus in a processor architecture, because processors can execute instructions and fetch data much faster than memories can be accessed to provide the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a system clock) associated with the programming engines; and

a pull bus arbiter (see Fig. 10, the PLB Arbiter) to arbitrate use of a unidirectional pull bus (see Fig. 10, wrDBus) by the external memory resources, the pull bus arbiter being internal to the data processor, the pull bus to pull data from an output transfer memory (not clearly shown by Correale, but it is clear that a register must be present on a processor's output port which is connected to a data bus in a processor architecture, because processors can execute instructions and provide read/write data much faster

than memories can be accessed to provide or store the data, and input/output registers are needed to synchronize the data transactions between a processor and a memory resource by using a clock) associated with the programming engines and to transfer the data to the memory resources.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7, 16-21, 26-29, 33-35, 37, 40, 41, 43-45, 50, 51, 53, 54 and 57-60 are rejected under U.S.C. 103(a) as being unpatentable over Correale and Shaylor [US 6,408,325 B1] (hereinafter "Shaylor").

Per claims 1, 26 and 37, it is clear the Correale already teaches most of the claims as described above (the programming agent in claim 56 is considered to be equivalent to the processing agent of claim 1), and further teaches issuing a write command (the pulling of data from the processing agent to the memory resources must be a result of a write command) and loading data into an output transfer memory of the processing agent (see the rejection of claims 13, 49, 55, 56 and 61 above). Correale

also discloses setting the output transfer memory to a read-only state, even though it does not explicitly recite this limitation. However, It should be clear that since processors can execute instructions and issue memory write request much faster than the actual write operations can be completed by accessing the much slower memory, the processor's output register must have its write enable control signal disabled while the data to be written to memory is ready to be transferred over the data bus, in order to avoid the data being overwritten by a new write data generated by the processor before the current transfer is complete.

Correale does not teach executing a context. Shaylor teaches a multi-tasking and multi-threading processor that can enhance data processing efficiency (see Shaylor, col. 1, lines 46-50), the processor requires executing a context for each thread (see Shaylor, col. 1, lines 56-67). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine the teachings of Shaylor and Correale, in order to enhance data processing efficiency. As a result of the combination, Correale and Shaylor in combination teach "executing a context".

Per claims 2, 16 and 27, the combined teaching of Correale and Shaylor further discloses establishing a plurality of contexts (see Shaylor, col. 1, lines 56-67) on the processing agent and maintaining program counters (although not specified in Shaylor, it is clear that in a multi-tasking and multi-threading processor taught by Shaylor, there must be multiple program counters for the concurrently executing processes and

threads) and context relative registers (see Shaylor col. 1, lines 20-32 and lines 56-67, col. 2, lines 1-27, col. 4, lines 37-67).

Per claims 3, 18, 28 and 50, the combined teaching of Correale and Shaylor further discloses the processing agent executes a context (see Shaylor, "context", col. 1, lines 56-67) and issues a read command to a memory controller in a read phase (see the rejection of claim 1 above, pushing data from the memory resources to the processing agent must be the result of a read command in a read phase).

Per claims 4 and 19, the combined teaching of Correale and Shaylor further discloses the memory controller processes the read command to be sent to one of the memory resources (see Correale, col. 5, lines 55-60, memory controller 704).

Per claims 5, 20, 29 and 51, the combined teaching of Correale and Shaylor further discloses the context is swapped out if the read data is required to continue the execution of the context (it is clear from the teaching of Shaylor that a context stores the state of a thread in memory and when a context switch occurs the context is saved to persistent storage, see Shaylor, col. 1, lines 56-67 and col. 2, lines 1-2; it is then further clear that if a read command issued by the thread requires data that is not stored in the memory that holds the context, then the context must be temporarily swapped out and stored in the persistent storage so that the context will not be overwritten by the acquired read data).

Per claim 6, the combined teaching of Correale and Shaylor further discloses after the memory controller has completed the processing of the read command, the memory controller pushes the data to an input transfer memory of the processing agent (see the rejection of claim 1 above for "input register").

Per claims 7 and 21, the combined teaching of Correale and Shaylor further discloses after the data has been pushed, the processing agent reads the data in the input transfer register (clearly the read data in the input register will be read by the processor) and the processing agent continues the execution of the context (see Shaylor, col. 1, lines 56-67, a context that was switched out must be switched back in to allow continued execution of the thread whose context was the switched out context).

Per claim 17, the combined teaching of Correale and Shaylor further discloses the context relative registers are selected from a group comprising of general purpose registers, inter-programming agent registers, static random access memory (SRAM) input transfer registers, dynamic random access memory (DRAM) input transfer registers, SRAM output transfer registers, DRAM output transfer registers, and local memory registers (see Shaylor, col. 1, lines 20-32 and lines 56-67, col. 2, lines 1-27, col. 4, lines 37-67).

Per claims 33, 40 and 54, the combined teaching of Correale and Shaylor further teaches the context is swapped out if the write command is required to continue the execution of the context (it is clear from the teaching of Shaylor that a context stores the state of a thread in memory and when a context switch occurs the context is saved to persistent storage, see Shaylor, col. 1, lines 56-67 and col. 2, lines 1-2; it is then further clear that if a write command issued by the thread writes to the memory storing the context, then the context must be temporarily swapped out and stored in the persistent storage so that the context will not be overwritten by the write command).

Per claims 34 and 41, the combined teaching of Correale and Shaylor further discloses the memory controller pulls the data from the output transfer memory and the memory controller sends a signal to the processing agent to unlock the output transfer memory (following the discussion in the rejection of claim 1 above, if the output register is write disabled, then it must be re-enabled in order for future write data to be stored by the processor).

Per claim 35, the combined teaching of Correale and Shaylor further discloses if the context has been swapped out after the output transferred memory has been unlocked, the context is swapped back in and the processing agent continues the execution of the thread (Shaylor teaches a swapped out context must be switched back in to continue the thread's execution, since claim 34 teaches the swapping out is the result of a write command's possibility of overwriting the context, then it is clear that the

context should be switched back in since re-enabling the output register indicates the write command is already completed).

Per claim 43-45, Correale further teaches the memory resources comprise memory controller channels (see Correale, col. 5, lines 54-60, memory controller 704 and PCI bridge 705).

Per claim 53, it is clear the claim is disclosed by claims 1, 26, 37 and 49 set forth above.

Per claims 57, 59 and 60, it is clear the claims are already disclosed by claims 1, 13, 49, 55, 56 and 61 as set forth above.

Per claim 58, it is clear the claim is already disclosed by claims 1, 13, 49, 55, 56 and 61 as set forth above.

Response to Arguments

7. Applicant's arguments with respect to claims 1-7, 13, 16-21, 26-29, 33-35, 37, 40, 41, 43-45, 49-51 and 53-61 have been considered but are not persuasive.

Regarding the Applicant's first argument (see Remarks, page 2, "First reason"), the Applicant is respectfully reminded that a PCI bridge qualifies as a memory resource under the broadest reasonable interpretation of the term, as a PCI bridge contains at

least buffers which store/memorizes data. Also, it should be reasonably clear that if Correale's slaves contain data to be read by masters and are capable of being written to by masters, then the slaves must contain some type of memory storage and the read/write data must be stored, however briefly, on the slaves. Therefore, Correale's slaves anticipate the Applicant's limitation under the broadest reasonable interpretation of the term "memory resource".

The Applicant's second argument (see Remarks, page 2, "Second reason") appears to be based on the reasoning in the Applicant's first argument ("First reason"), which has been traversed as set forth above. The Applicant further argues (see Remarks, page 3, first paragraph) that Correale does not disclose an arbiter that arbitrates requests from the slave devices and arbitrating use of the data buses by the memory resources. However, the issue at hand is arbitration of the read bus, not from whom or where the requests are generated since the claims do not state this feature. Furthermore, Correale clearly teaches read bus arbitration and arbitrating use of the data buses by the slaves (all uses of the data buses by the slaves are either directly or indirectly resulted from some arbitration, see Fig. 8; also see col. 6, liens 29-40 and col. 4, lines 38-39, also see the response to Applicant's third argument below).

Regarding the Applicant's third argument (see Remarks, last two paragraphs on page 3 to page 4) that Correale does not disclose "the memory resources obtaining access to the pull bus based on arbitration by the pull bus arbiter", the Applicant is respectfully reminded that the claims do not state that it is necessarily the memory resources that compete for bus access through arbitration, instead the claims merely

state the memory resources "obtain" access to a pull bus "based on" an arbitration. This implies the obtaining can be achieved directly or indirectly based on an arbitration. Correale teaches writes are arbitrated (see col. 4, lines 38-39, also see Figs. 9 and 10). The pull bus includes the entire length of wrDBus from masters to slaves. Hence, for a write to complete, the target slave must obtain access to the segment of wrDBus between the writing master and the multiplexer on the write bus wrDBus inside the PLB arbiter to receive the write data. Similar reasoning is applied to the other assertion that Correale does not disclose "the memory resources obtaining access to the push bus based on arbitration by the push bus arbiter" (push bus is the read bus rdDBus).

Conclusion

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

9 December 2007

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
12/13/07